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- 1. (amended) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;
- a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads,
  - a low dielectric constant sheath surrounding each wire, and
  - a mold compound encasing the chip, sheathed wires, and leads.

 $a^2$ 

- 10. (amended) A device as in claim 1 wherein said device is packaged in a Ball Grid Array package.
- 11. (amended) A device as in claim 1 wherein said device is packaged as a leaded surface mount package.

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- 14. (amended) A device as in claim 1 wherein said cavity package shell comprises a ceramic.
- 16. (amended) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of wire bonds connecting pads on an integrated circuit chip to conductive leads,

a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads.

17. (cancelled without prejudice).